IN THE SPECIFICATION:

Please substitute paragraph **[0001]** with the following:

[0001] This application is a continuation of application Serial No. 09/777,986, filed February 6, 2001, now U.S. Patent 6,340,302, issued January 22, 2002.

IN THE CLAIMS:

Claim10 has been amended herein. All of the pending claims 1 through 20 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Attached is a marked-up version of the claims amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

1. A method for establishing an electrical contact with at least one semiconductor device, comprising:

establishing an electrical contact between a first member of an electrical connector and a contact that is in electrical communication with the at least one semiconductor device; and

drawing said first member toward said contact.

2. The method of claim 1, wherein said drawing is effected in a direction substantially normal to a plane of said contact.

3. The method of claim 1, wherein said drawing is effected in a direction substantially normal to a plane of a substrate upon which said contact is carried.

4. The method of claim 1, wherein said drawing is effected by positioning a second member of said electrical connector opposite said first member.

5. The method of claim 4, wherein said drawing is effected by magnetically attracting at least one of said first member and said second member toward at least the other of said first member and said second member.

6. The method of claim 4, wherein said drawing comprises securing said first and second members to a substrate upon which said contact is carried.

7. The method of claim 1, wherein said drawing comprises magnetically attracting said first member against said contact.

8. A method for stress testing a plurality of semiconductor devices carried upon a common substrate and in communication with common ground and power contacts, comprising:
establishing electrical contact between a first member of an electrical connector and at least one contact of the ground contact and the power contact; and
drawing said first member toward said at least one contact.

9. The method of claim 8, wherein said drawing is effected in a direction substantially normal to a plane of the substrate.

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10. (Amended) The method of claim 8, wherein said drawing nonrigidly biases said first member against said at least one contact.

11. The method of claim 8, wherein said drawing comprises positioning a second member of said electrical connector opposite the substrate from said first member.

12. The method of claim 11, wherein at least one of said first member and said second member is drawn toward at least the other of said first member and said second member.

13. The method of claim 12, wherein said drawing comprises magnetically attracting at least one of said first member and said second member toward at least the other of said first member and said second member.

14. The method of claim 8, wherein said drawing comprises magnetically attracting said first member against said at least one contact.

15. The method of claim 8, wherein said drawing comprises securing at least said first member in position relative to the substrate.

16. The method of claim 8, further comprising:

electrically connecting another first member of another electrical connector to another of the ground contact and the power contact; and

drawing said another first member toward said another contact.

17. The method of claim 16, further comprising:

applying a substantially constant amount of current to each semiconductor device of the plurality of semiconductor devices through said first member and said another first member.

18. The method of claim 17, further comprising:

heating each of the plurality of semiconductor devices.

19. The method of claim 18, wherein said heating comprises cycling a temperature of each of the plurality of semiconductor devices.

20. The method of claim 18, wherein said heating comprises varying a temperature of each of the plurality of semiconductor devices.